Integrated High Voltage CMOS Charge Pump

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**Motivation & Objectives**
- The dynamically reconfigurable transceiver architecture in LOEWE Project Cocoon requires an innovative integrated control circuit.
- The generation of high voltage provided from available low voltage rechargeable batteries with typically 3.7V DC is becoming an important issue

*Special features:*
- monolithic, high voltage generation, energy efficiency, robustness, costs

**Methods / Approach**
- Proposed 4-Phase Charge Pump Architecture
- 4-Phase Clock Scheme

- Improved circuit based on Pelliconi charge pump
- Dynamical biasing of bulk terminals of MOS-switches
- Dead time technique at the clock scheme to reduce reverse current problem

0.35 um High Voltage CMOS Technology H35 of Austriamicrosystems

- Isolated LV Transistors with HV offset. HV Sandwich Capacitors.
- \( V_{DDP} \) is maximal 120 V. Triple well CMOS process.

**Simulation Results**

Two configurations of the HV sandwich capacitors:
- **config.1:** deep NWELL connected with one terminal of the capacitor and clock buffers.
- **config.2:** deep NWELL connected with one terminal of the capacitor, but not with clock buffers.

Total layout size of the chip using **config.1:** 3.9 X 5.6 mm².

Schematic simulations including clock buffers are under the following conditions: stage number \( N = 36 \), \( Vdd = Vclk = 3.7V \), \( f = 10MHz \), \( C_{pumping} = 10pF \), \( C_{load} = 30pF \), \( R_{load} = 1.05M \). For the proposed charge pump additionally: \( C_{control} = 78fF \), dead time \( T2 = T4 = 8ns \), charge transfer time \( T1 = T3 = 42ns \).

<table>
<thead>
<tr>
<th>36 Stage Charge Pump Circuits</th>
<th>( Vout(V) )</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pelliconi Config.1</td>
<td>90</td>
<td>13 %</td>
</tr>
<tr>
<td>Pelliconi Config.2</td>
<td>84</td>
<td>26 %</td>
</tr>
<tr>
<td>Proposed charge pump Config.1</td>
<td>116</td>
<td>21 %</td>
</tr>
<tr>
<td>Proposed charge pump Config.2</td>
<td>105</td>
<td>39 %</td>
</tr>
</tbody>
</table>

**Measurement Results**

Two-phase clock scheme is realized by setting dead time \( T2 = T4 = 0ns \). The measurement condition is similar to the simulation conditions.

<table>
<thead>
<tr>
<th>Frequency(MHz)</th>
<th>( Vdd/Vclk(V) )</th>
<th>( Idma(\mu A) )</th>
<th>( Vout(V) )</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>3</td>
<td>21.7</td>
<td>84.5</td>
<td>11%</td>
</tr>
<tr>
<td>10</td>
<td>2.2</td>
<td>25.6</td>
<td>91.3</td>
<td>10.7%</td>
</tr>
<tr>
<td>10</td>
<td>5.7</td>
<td>26.4</td>
<td>97.3</td>
<td>9.9%</td>
</tr>
</tbody>
</table>

Measurement results using 2-phase clock

<table>
<thead>
<tr>
<th>Frequency(MHz)</th>
<th>( Vdd/Vclk(V) )</th>
<th>( Idma(\mu A) )</th>
<th>( Vout(V) )</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>5</td>
<td>21.4</td>
<td>87.2</td>
<td>11.8%</td>
</tr>
<tr>
<td>10</td>
<td>3.3</td>
<td>23.5</td>
<td>95.4</td>
<td>11.7%</td>
</tr>
<tr>
<td>10</td>
<td>1.7</td>
<td>26.3</td>
<td>106</td>
<td>11.5%</td>
</tr>
</tbody>
</table>

Measurement results using 4-phase proposed clock

The proposed charge pump architecture with 4-phase clock scheme shows better performance than that of the traditional 2-phase non-overlapping Pelliconi charge pump. The ramp-up time is approx. 96.4ns, which is slower than the simulated 130μs.